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10/690,560	10/23/2003	Hideki Nakahara	2003_1514A	6440

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EXAMINER	
BENGHUZZI, MOHSIN M	
ART UNIT	PAPER NUMBER
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)
	10/690,560	NAKAHARA ET AL.
	Examiner	Art Unit
	Mohsin (Ben) Benghuzzi	2611

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *23 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,13 and 15-20* is/are rejected.

7)☒ Claim(s) *11,12 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *23 October 2003* / 8 April, 2004 / 26 Oct. 2004 M.B
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10, 13 and 15-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhou et al. (US 6,278,724) in view of Nakamura et al. (US 7,023,940).

1) Regarding claim 1:

Zhou et al. discloses a phase error correction circuit for correcting a phase error in an input signal having a frame structure containing a preamble, a specific pattern, and data, comprising:

a correction value calculation section for calculating a phase correction value based on a predetermined number of symbols contained in the input signal (column 11 line 61 to column 12 line 6 and column 7 lines 1-16);

a correction value determination section for retaining with a predetermined timing a phase correction value calculated by the phase correction value calculation section, based on the predetermined number of symbols contained in the preamble (column 11 line 61 to column 12 line 6 and column 7 lines 1-16, wherein, the 'correction vector generator' is interpreted as the correction value determination section);

a phase rotation section for subjecting the input signal to a phase rotation process using the phase correction value retained in the correction value determination section (column 3 lines 3-8, column 5 lines 4-8, and column 30 line 58 to column 31 line 38, wherein, phase rotation as disclosed in the instant application is interpreted from eq. 1 and eq. 2 on page 25 of specification, and the 'phase corrector' of Fig. 18 in Zhou et al. is interpreted as the phase rotation section);

wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section with a timing determined based on the specific pattern detection signal (column 29 lines 36-40 and column 7 lines 11-14, wherein, the 'refreshable time interval' is interpreted as the determined timing).

Zhou et al. does not disclose, a specific pattern detection section for detecting the specific pattern contained in an output signal from the phase rotation section to output a specific pattern detection signal. However, Nakamura et al. discloses, a specific pattern detection section for detecting the specific pattern contained in an output signal from the phase rotation section to output a specific pattern detection signal (column 18 lines 20-31).

It is desirable that, in a phase error correction circuit, a specific pattern detection section is employed for a specific pattern contained in the received signal. Detection of a specific pattern allows for clock synchronization from the received signal (see Zhou et al., column 18 lines 24-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include in the phase error correction

circuit of Zhou et al. a specific pattern detection section, as Nakamura et al. teaches, in order to allow for lock synchronization from the received signal.

2) Regarding claim 2:

Zhou et al. discloses the phase error correction circuit according to claim 1, wherein,

the correction value determination section outputs the phase correction value calculated by the correction value calculation section to the phase rotation section until retaining the phase correction value calculated by the correction value calculation section with the predetermined timing (column 11 line 61 to column 12 line 6, column 7 lines 1-16, and column 30 line 58 to column 31 line 38, wherein, the 'refreshable time interval' is interpreted as the predetermined timing and the 'phase corrector' of Fig. 18 is interpreted as the phase rotation section), and

until the correction value determination section retains the phase correction value calculated by the correction value calculation section with the predetermined timing, the phase rotation section subjects the input signal to a phase rotation process using the phase correction value which is output from the correction value determination section (column 11 line 61 to column 12 line 6, column 7 lines 1-16, and column 30 line 58 to column 31 line 38, wherein, the 'refreshable time interval' is interpreted as the predetermined timing and the 'phase corrector' of Fig. 18 is interpreted as the phase rotation section).

3) Regarding claim 3:

Zhou et al. discloses the phase error correction circuit according to claim 1, further comprising an alternation detection section for outputting an alternation detection signal indicating inversions of a sign of the input signal from symbol to symbol (column 7 lines 34-40).

4) Regarding claim 4:

As discussed in claim 1, Zhou et al. discloses the phase error correction circuit according to claim 3, wherein the correction value calculation section calculates the phase correction value (column 11 line 61 to column 12 line 6 and column 7 lines 1-16). Regarding, with respect to a portion of the input signal for which the alternation detection signal is output, Nakamura et al. teaches, with respect to a portion of the input signal for which the alternation detection signal is output (column 3 lines 20-43).

5) Regarding claim 5:

Zhou et al. discloses the phase error correction circuit according to claim 1, wherein

the correction value calculation section (column 11 line 61 to column 12 line 6 and column 7 lines 1-16) includes:

a phase inversion section for inverting a phase of the input signal from symbol to symbol (column 7 lines 34-40);

a mean value inversion section for inverting, depending on a sign of an output signal from the mean value calculation section, the sign of the output signal (column 7 lines 34-40).

Zhou et al. does not disclose, a mean value calculation section for calculating a mean value of the predetermined number of symbols in an output signal from the phase inversion section. However, Nakamura et al. disclose, a mean value calculation section for calculating a mean value of the predetermined number of symbols in an output signal from the phase inversion section (column 12 lines 55-64, wherein, it is understood that an 'average value' is equivalent to a mean value).

It is well known in the art that using a mean value of a number of symbols results in more accurate calculation, and thus, in a more accurately detected output signal. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the mean value calculation section of Nakamura et al. in the phase error correction circuit of Zhou et al., in order to result in a more accurately detected output signal.

6) Regarding claim 6:

Nakamura et al. discloses, wherein the mean value calculation section calculates the mean value by cumulatively adding the output signal from the phase inversion section by using one symbol adder, such that one mean value is calculated per plurality of symbol periods (column 12 lines 51-54).

7) Regarding claim 7:

Nakamura et al. discloses, wherein the mean value calculation section calculates the mean value by cumulatively adding the output signal from the phase inversion section by using a plurality of symbol adders in parallel, such that one mean value is calculated per symbol period (column 12 lines 46-54, wherein, it is interpreted that since

the serial/parallel converter, bock 37 in Fig. 4, converts serial data to parallel data and outputs the parallel data to the adder, block 38, the adder must then be comprised of a plurality of adders in parallel).

8) Regarding claim 8:

Zhou et al. discloses the phase error correction circuit according to claim 7, further comprising a delay section for delaying the input signal supplied to the correction value calculation section by a predetermined amount of time from the input signal supplied to the phase rotation section (26 in Fig. 2 and column 30 lines 24-30).

As discussed in claim 1 above, Nakamura et al. discloses, wherein the predetermined amount of time is determined so that the specific pattern is detected by the specific pattern detection section while the correction value calculation section is calculating the phase correction value with respect to the preamble contained in the input signal (column 18 lines 20-31).

9) Regarding claim 9:

Zhou et al. discloses the phase error correction circuit according to claim 1, wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section based on the predetermined number of symbols including the last symbol of the preamble (column 7 lines 3-16, wherein, the 'information symbol block' is interpreted as the predetermined number of symbols).

10)Regarding claim 10:

Zhou et al. discloses the phase error correction circuit according to claim 1, wherein the correction value determination section includes:

a correction value storage section for storing a plurality of phase correction values calculated by the correction value calculation section in a chronological order (column 29 lines 36-39);

Zhou et al. does not specifically disclose a correction value selection section for selecting one of the phase correction values stored in the correction value storage section, however, it should be obvious to one of ordinary skill in the relevant art that from a set of phase correction values, one value must be selected for phase correction, in order for the phase correction to be performed. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a correction value selection section in the phase error correction circuit of Zhou et al. in order to be able to select a phase correction value that is needed to perform phase error correction.

As discussed in claim 1 above, Nakamura et al. discloses, a correction value retention section for, based on the specific pattern detection signal, fetching and retaining the phase correction value selected by the correction value selection section, and stopping fetching the phase correction value after the specific pattern detection signal is output.

11)Regarding claim 13:

As discussed in claim 1 above, Nakamura et al. discloses, wherein the correction value determination section stops fetching the phase correction value after the specific pattern detection signal is output (column 18 lines 20-31, wherein, 'establishes clock synchronization' is interpreted to indicate the correction value determination section stops fetching the phase correction value).

12)Regarding claim 15:

Although Zhou et al. doesn't specifically disclose, further comprising a 45° rotation section for rotating a phase of the input signal supplied to the correction value calculation section by 45°, such limitation is merely a matter of design choice and would have been obvious in the system of Zhou et al. The amount of rotation inserted prior to the phase error correction circuit is dependent on the type of transmitter modulation method. The amount of angle rotation and whether a rotation is needed at all depends on how the correction value calculation section is designed. As it is the case in the instant application, if the correction value calculation section is designed to accommodate a QPSK modulation, a 45° angle rotation is then needed. On the other hand, if the correction value calculation section is designed to match the type of the transmitted modulation method, an angle rotation is then not needed. Therefore, to have a 45° rotation section in Zhou et al.'s phase error correction circuit for rotating a phase of the input signal supplied to the correction value calculation section by 45° would have been a matter of obvious design choice to one of ordinary skill in the art.

13)Regarding claim 16:

Zhou et al. discloses a receiver for receiving a digitally-modulated signal, comprising:

a detector section for detecting a received signal (Abstract lines 3-5);

a clock recovery section for recovering a clock signal from an output signal from the detector section while switching zero cross reference axes based on a given control signal (column 18 lines 20-28, wherein, the 'sampling clock' is interpreted as the clock signal); and

a phase error correction circuit for correcting a phase error in an output signal from the detector section for which judging points have been determined based on the clock signal recovered by the clock recovery section, and supplying phase error information indicating a magnitude of the phase error as the control signal to the clock recovery section (31, 35, 40 in Fig. 2, column 11 line 61 to column 12 line 6, column 7 lines 1-16, and column 30 line 58 to column 31 line 38).

14)Regarding claim 17:

Zhou et al. discloses the receiver according to claim 16, wherein,

the received signal is a signal having a frame structure containing a preamble and data (Fig. 13 a), and

the phase error correction circuit comprises:

a correction value calculation section for calculating a phase correction value based on a predetermined number of symbols contained in the output signal from the detector section (column 11 line 61 to column 12 line 6 and column 7 lines 1-16);

a correction value determination section for retaining with a predetermined timing a phase correction value calculated by the phase correction value calculation section, based on the predetermined number of symbols contained in the preamble (column 11 line 61 to column 12 line 6 and column 7 lines 1-16, wherein, the 'correction vector generator' is interpreted as the correction value determination section);

a phase rotation section for subjecting the output signal from the detector section to a phase rotation process using the phase correction value retained in the correction value determination section (column 3 lines 3-8, column 5 lines 4-8, and column 30 line 58 to column 31 line 38, wherein, phase rotation as disclosed in the instant application is interpreted from eq. 1 and eq. 2 on page 25 of specification, and the 'phase corrector' of Fig. 18 in Zhou et al. is interpreted as the phase rotation section);

wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section with a timing determined based on the specific pattern detection signal (column 29 lines 36-40 and column 7 lines 11-14, wherein, the 'refreshable time interval' is interpreted as the determined timing).

Furthermore, as discussed in claim 1 above, Nakamura et al. discloses, a specific pattern, and a specific pattern detection section for detecting the specific pattern contained in an output signal from the phase rotation section to output a specific pattern detection signal (column 18 lines 20-31).

15)Regarding claim 18:

Zhou et al. discloses a receiver for receiving a digitally-modulated signal, comprising:

a detector section for detecting a received signal (Abstract lines 3-5);

a phase error correction circuit for correcting a phase error in an output signal from the detector section using a given clock signal (31, 35, 40 in Fig. 2, column 11 line 61 to column 12 line 6, column 7 lines 1-16, and column 30 line 58 to column 31 line 38); and

a clock recovery section for, based on a signal which has been corrected by the phase error correction circuit, recovering a clock signal to be used for demodulating the signal, and supplying the recovered clock signal to the phase error correction circuit (column 18 lines 20-28, wherein, the 'sampling clock' is interpreted as the clock signal).

16)Regarding claim 19:

Zhou et al. discloses the receiver according to claim 18, wherein,

the received signal is a signal having a frame structure containing a preamble and data (Fig. 13 a), and

the phase error correction circuit comprises:

a correction value calculation section for calculating a phase correction value based on a predetermined number of symbols contained in the output signal from the detector section (column 11 line 61 to column 12 line 6 and column 7 lines 1-16);

a correction value determination section for retaining with a predetermined timing a phase correction value calculated by the phase correction value calculation section,

based on the predetermined number of symbols contained in the preamble (column 11 line 61 to column 12 line 6 and column 7 lines 1-16, wherein, the 'correction vector generator' is interpreted as the correction value determination section);

a phase rotation section for subjecting the output signal from the detector section to a phase rotation process using the phase correction value retained in the correction value determination section (column 3 lines 3-8, column 5 lines 4-8, and column 30 line 58 to column 31 line 38, wherein, phase rotation as disclosed in the instant application is interpreted from eq. 1 and eq. 2 on page 25 of specification, and the 'phase corrector' of Fig. 18 in Zhou et al. is interpreted as the phase rotation section);

wherein the correction value determination section retains the phase correction value calculated by the correction value calculation section with a timing determined based on the specific pattern detection signal (column 29 lines 36-40 and column 7 lines 11-14, wherein, the 'refreshable time interval' is interpreted as the determined timing).

Furthermore, as discussed in claim 1 above, Nakamura et al. discloses, a specific pattern, and a specific pattern detection section for detecting the specific pattern contained in an output signal from the phase rotation section to output a specific pattern detection signal (column 18 lines 20-31).

17)Regarding claim 20:

Zhou et al. teaches a signal transmission method for transmitting data in frames, comprising the steps of:

splitting data to be transmitted into units of a predetermined length (P1, D1 to P4, D4 in Fig. 13a, wherein, each of the combination of P, D is interpreted as a unit of predetermined length. Also, see column 1 lines 38-53);

subjecting the frame-structured data to digital modulation and transmitting the modulated frame-structured data (P1, D1 to P4, D4 in Fig. 13a, wherein, each of the combination of P, D is interpreted as a unit of predetermined length. Also, see column 1 lines 38-53, wherein, BPSK or QPSK is understood to be the digital modulation).

Furthermore, Nakamura et al. discloses, generating a frame-structured data by adding, in front of each unit of split data, a preamble which alternates from symbol to symbol, and a specific pattern selected so as not to allow a predetermined length of symbol-to-symbol alternations to occur even in the presence of a symbol error (column 3 lines 20-43).

Allowable Subject Matter

3. Claims 11, 12, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to clearly teach or suggest the correction value selection section receives an indication of a number of correction values to go back, and selects and outputs a phase correction value after a predetermined amount of time since the end detection signal is output.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Inagawa (US 6,334,203) discloses an error detecting method and device for calculating phase error in a PSK modulated signal.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohsin (Ben) Benghuzzi whose telephone number is (571) 270-1075. The examiner can normally be reached Monday through Friday, 8:30am- 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mohsin (Ben) Benghuzzi February 23, 2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER